Download Digital Logic Design Interview Questions And Answers

There are no predefined Digital design interview questions as the person can ask anything starting from a simple concept to advance level and it also varies at different experience level.Designer must how data flows between various registers of the design.Gate level: The module is implemented in terms of logic gates and interconnections between these gates. Designer should know the gate-level diagram of the design.Switch level: This is the lowest level of abstraction. The design is implemented using switches/transistors. Designer requires the knowledge of switch-level ...Digital Logic Design VIVA Questions and Answers :- 1) Explain about setup time and hold time, what will happen if there is setup time and hold tineDigital design interview questions & answers. 1) Explain about setup time and hold time, what will happen if there is setup time and hold tine violation, how to overcome this? Set up time is the amount of time before the clock edge that the input signal needs to be stable to guarantee it is accepted properly on the clock edge.